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Feb 22, 2019 KiCad release 5.0.1 stable comes with over a dozen fixes and minor improvements. Mainly to work around the main issue with KiCad 5.0 where the .1. Field of the Invention This invention generally relates to semiconductor devices and more particularly to integrated circuits having active layers that are configured with a lattice that includes a strain-engineered substrate. 2. Description of the Related Art There are two principal methods for producing high performance CMOS integrated circuits, including microprocessors, static random access memories (SRAMs), and logic integrated circuits: 1) the semiconductor substrate and the integrated circuits are formed from silicon (Si), and 2) the integrated circuits are formed on strained silicon/germanium (Si/Ge) material. In the first method, because Si is used for the integrated circuit, the substrate is a bulk Si wafer. In the second method, a thick layer of relaxed Si/Ge is used as a substrate for the integrated circuits, rather than a silicon wafer. The Si/Ge film is relaxed because of a lattice mismatch between Si and Ge, and this creates a built-in strain in the Si/Ge layer that is desirable for increasing the mobility of electrons and holes in the Si/Ge layer. In the conventional CMOS structure described above, gate stacks are fabricated on both sides of the Si/Ge substrate. The substrate and the gates are encapsulated using a nitride-based dielectric material, and a buried oxide (BOX) layer is used to separate the substrate from adjacent layers of circuits. In the case of Si/Ge structures, the buried oxide (BOX) layer is also replaced by a strain-inducing SiGe layer located between the Si/Ge substrate and the Si/Ge epitaxial layer. The SiGe substrate improves the strain in the Si/Ge epitaxial layer and also improves the mobility of electrons and holes in Si/Ge devices. However, because the C—H bonds in Si/Ge are stronger than the Si—Si bonds, some damage occurs when the CMOS structure is exposed to an oxidizing ambient at a relatively high temperature, such as in a typical CMOS manufacturing process. When this oxidation occurs, the SiGe nitride material bonds preferentially to the Si/Ge material and the thickness of the SiGe layer is reduced. A similar effect results when the CMOS structure is exposed to water during a CMP (

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